eFPGA Saved Us Millions of Dollars. It Can Do the Same for You.

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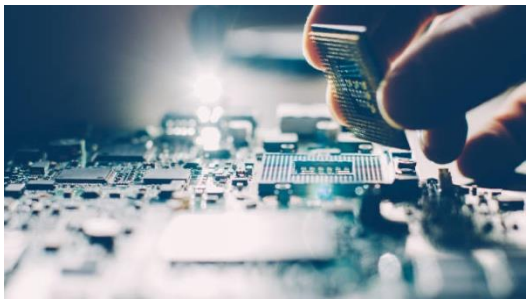
For those of you who follow Flex Logix®, you already know that we have an IP business, EFLX® eFGPA, and an edge inferencing co-processor chip and board business, InferX®. InferX came about because we had many customers ask if they can run AI/ML algorithms in EFLX. The answer was and still is, of course you can – EFLX is an FPGA fabric similar to what FPGA chips use. Our co-founder, Cheng Wang, took some time and studied the challenges of AI processing in more detail and came up with a highly efficient edge inferencing processor leveraging Flex Logix proprietary eFPGA technology. When performance, power and area results were shared with our board of directors, they thought it so compelling, they told us to build a chip. Hence, InferX X1 was born.

The X1 was specified to be a lean, high performance edge accelerator for AI inference processing incorporating Flex Logix' proprietary tensor processor, PCIe, DDR, memory and a NoC. When it came time to architect the chip, there was an internal debate about adding EFLX to the X1 chip, mainly because it takes up area and our use case was pretty basic: support a GPIO interface and help with chip debug. Not a strong reason to add one square millimeter in 16nm. We proceeded anyway to demonstrate "Eating our own dog food", by connecting the eFPGA to both the NoC bus and GPIO to maximize flexibility.



Fast forward to chip bring-up.

We ran into an issue whose immediate solution could not be resolved in software and was looking like we needed a partial re-spin that would cost us several million dollars in mask fees. With the team's creative thinking and hard work, they came up with a solution utilizing the eFPGA and adding functionality to the chip that wasn't conceived of or anticipated during chip definition and allowed us to meet our speed and functional specs as planned without any compromise. That one square millimeter of eFPGA saved us millions of dollars and avoided a delay of 6 – 9 months in sampling full speed chips

We are seeing more chips being architected with EFLX with specific use cases leveraging reconfigurability in mind (13 in silicon and another 11 in design). These applications vary from 5G, computational storage, vehicle-to-vehicle communications and MCUs to name a few. But for those folks architecting new chips who aren't sure how they would use eFPGA, carving a

little area for eFPGA could save millions of dollars, or more importantly, avoid missing a market window because you had to re-spin a chip.

Andy Jaros
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